I CLAIM:

1. A data processing apparatus comprising:

a master device;

a slave device; and

a communication bus operable to pass transaction requests from said master device to said slave device; wherein

said master device having a transaction annotator operable to generate a transaction identifier as part of each transaction request passed from said master device to said slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request; and

said slave device having transaction ordering logic operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers.

2. A data processing apparatus according to claim 1, in which said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device.

3. A data processing apparatus according to claim 2, in which said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

4. A data processing apparatus according to claim 1, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

5. A data processing apparatus according to claim 1, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

6. A data processing apparatus according to claim5, in which said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

7. A data processing apparatus according to claim 6, in which said slave device comprises logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

8. A data processing apparatus according to claim 1, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

9. A data processing apparatus according to claim 1, in which said transaction request is either a read request for reading data from a memory attached to said slave device or a write request for writing data to said memory attached to said slave device.

10. A data processing apparatus according to claim 1, in which said transaction identifier comprises a sequence of bit values and said slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

11. A data processing apparatus according to claim 1, in which said slave device is a memory controller.

12. A data processing apparatus according to claim 1, in which said master device is one of:

a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

13. A master device operable to pass transaction requests across a communication bus to a slave device, said master device comprising a transaction annotator operable to generate a transaction identifier as part of each transaction request passed from said master device to said slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request;

wherein said transaction identifier contains information enabling a slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers.

14. A master device according to claim 13, in which said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device.

15. A master device according to claim 12, in which said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

16. A master device according to claim 13, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

17. A master device according to claim 13, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

18. A master device according to claim 17, in which said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

19. A master device according to claim 18, in which said slave device comprises logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion to derive said timeout value.

20. A master device according to claim 13, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

21. A master device according to claim 13, in which said transaction request is either a read request for reading data from a memory attached to said slave device or a write request for writing data to said memory attached to said slave device.

22. A master device according to claim 13, in which said transaction identifier comprises a sequence of bit values and said slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

23. A master device according to claim 13, in which said slave device is a memory controller.

24. A master device according to claim 13, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

25. A slave device operable to receive transaction requests from a master device across a communication bus, said slave device having transaction ordering logic operable process a transaction identifier received from a master device as part of a transaction request, said transaction request having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction ordering logic being operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers.

26. A data processing apparatus according to claim 25, in which said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device.

27. A slave device according to claim 26, in which said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

28. A slave device according to claim 25, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

29. A slave device according to claim 25, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

30. A slave device according to claim 25, in which said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

31. A slave device according to claim 30, comprising logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

32. A slave device according to claim 25, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

33. A slave device according to claim 25, in which said transaction request is either a read request for reading data from a memory attached to said slave device or a write request for writing data to said memory attached to said slave device.

34. A slave device according to claim 25, in which said transaction identifier comprises a sequence of bit values and said slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

35. A slave device according to claim 25, in which said slave device is a memory controller.

36. A slave device according to claim 25, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

37. A bus carrying a transaction request signal from a master device to a slave device, said transaction request signal comprising a transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction identifier enabling a slave device to determine an order of service of a plurality of transaction requests having respective

transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers.

38. A bus according to claim 37, in which said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device.

39. A bus according to claim 37, in which said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

40. A bus according to claim 37, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

41. A bus according to claim 37, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

42. A bus according to claim 41, in which said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

43. A bus according to claim 42, in which said timeout value is derived by said slave device using logic to select a subset of bits of said master identifier portion to be concatenated with said priority portion to derive said timeout value.

44. A bus according to claim 37, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

45. A bus according to claim 37, in which said transaction request is either a read request for reading data from a memory attached to said slave device or a write request for writing data to said memory attached to said slave device.

46. A bus according to claim 37, in which said transaction identifier comprises a sequence of bit values and said slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

47. A bus according to claim 37, in which said slave device is a memory controller.

48. A bus according to claim 37, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

49. A data processing method for passing transaction requests from a master device to a slave device across a communication bus, said method comprising the steps of:

generating in a master device a transaction identifier as part of each transaction request passed from said master device to said slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request; and

determining at said slave device an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers.

50. A data processing method according to claim 49, in which said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device.

51. A data processing method according to claim 49, in which said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

52. A data processing method according to claim 49, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

53. A data processing method according to claim 49, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier..

54. A data processing method according to claim 53, in which said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

55. A data processing method according to claim 54, in which said slave device comprises logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

56. A data processing method according to claim 49, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

57. A data processing method according to claim 49, in which said transaction request is either a read request for reading data from a memory attached to said slave

device or a write request for writing data to said memory attached to said slave device.

58. A data processing method according to claim 49, in which said transaction identifier comprises a sequence of bit values and said slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

59. A data processing method according to claim 49, in which said slave device is a memory controller.

60. A data processing method according to claim 49, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

61. A method of generating in a master device, transaction requests for sending across a communication bus to a slave device, said method comprising the step of :

generating a transaction identifier as part of each transaction request passed from said master device to said slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request;

wherein said transaction identifier contains information enabling a slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers.

62. A method according to claim 61, in which said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device.

63. A method according to claim 61, in which said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

64. A method according to claim 61, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

65. A method according to claim 61, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

66. A method according to claim 65, in which said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

67. A method according to claim 61, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

68. A method according to claim 61, in which said transaction request is either a read request for reading data from a memory attached to said slave device or a write request for writing data to said memory attached to said slave device.

69. A method according to claim 61, in which said transaction identifier comprises a sequence of bit values and said slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

70. A method according to claim 61, in which said slave device is a memory controller.

71. A method according to claim 61, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

72. A method of controlling a slave device to service transaction requests received from a master device across a communication, said method comprising the step of:
processing a transaction identifier received from a master device as part of a transaction request, said transaction request having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction ordering logic being operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers.

73. A method according to claim 72, in which said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device.

74. A method according to claim 73, in which said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

75. A method according to claim 72, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

76. A method according to claim 72, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

77. A method according to claim 76, in which said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

78. A method according to claim 77, in which said slave device comprises logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

79. A method according to claim 72, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

80. A method according to claim 72, in which said transaction request is either a read request for reading data from a memory attached to said slave device or a write request for writing data to said memory attached to said slave device.

81. A method according to claim 72, in which said transaction identifier comprises a sequence of bit values and said slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

82. A method according to claim 72, in which said slave device is a memory controller.

83. A method according to claim 72, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

84. A method of transmitting a transaction request on a bus comprising the steps of:

generating a transaction request signal comprising a transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction identifier enabling a slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers; and

transmitting said transaction request signal across said bus.

85. A method according to claim 84, in which said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device.

86. A method according to claim 85, in which said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

87. A method according to claim 84, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

88. A method according to claim 84, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

89. A method according to claim 84, in which said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

90. A method according to claim 89, in which said slave device comprises logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

91. A method according to claim 84, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

92. A method according to claim 84, in which said transaction request is either a read request for reading data from a memory attached to said slave device or a write request for writing data to said memory attached to said slave device.

93. A method according to claim 84, in which said transaction identifier comprises a sequence of bit values and said slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

94. A method according to claim 84, in which said slave device is a memory controller.

95. A method according to claim 84, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.